**Lab 8**

**Objectives:**

∙ To learn the implementation of Boolean function using multiplexer ∙ To learn how to implement Multiplexers using decoders

**2-to-4 line decoders:**

74LS139 IC contains two fully independent 2-to-4 line decoders with active low enables. The function table and connection diagram for this IC are shown below:

**Function Table:**

| **Enable** | **Selection**  **Inputs** | | **Outputs** | | | |
| --- | --- | --- | --- | --- | --- | --- |
| **G** |  | **B** |  | **A Y0 Y1** |  | **Y2** |
| H |  | X |  | X H |  | H H |
| L |  | L | L | L | H | H |
| L |  | L | H | H |  | L H |
| L |  | H |  | L H |  | H L |
| L |  | H |  | H H |  | H H |

**Y3**

H

H

H

H

L

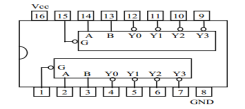
H= Logic High, L= Logic Low, X= Don’t Care

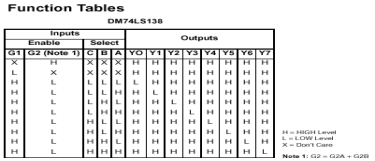
**Connection Diagram:**

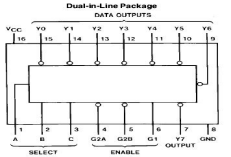
**3-to-8 line decoders:**

74LS138 IC contains 3-to-8 line decoder. The function table and connection diagram for this IC

are shown below:



**Connection Diagram:**

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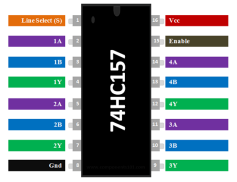
**2x1 MUX:**

74LS157 IC has 2 data input lines and 1 select line. The state of select line decides which of the inputs propagates to the output.

| **S** |  |
| --- | --- |
| **0** |  |
| **1** |  |

**Y Io**

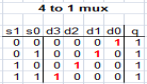
**I1**

****

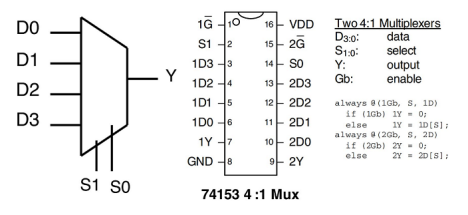
**4x1 MUX:**

74LS153 IC is 4x1 Multiplexer has four data inputs d3, d2, d1 & d0, two selection lines s1 & s0 and one output q. The function table and connection diagram for this IC are shown below:

**Function Table:**

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**Connection Diagram:**

 **Half Adder:**

Half adder is a logic circuit that performs binary addition of two 1-bit numbers. It generates two outputs namely ‘**Sum**’ and ‘**Carry**’.

**Truth Table:**

| **A** |  | **BCarry** | **Su**  **m** |
| --- | --- | --- | --- |
| 0 |  | 0 | 0 |
| 0 |  | 1 | 0 |
| 1 |  | 0 | 0 |
| 1 |  | 1 | 1 |

**Boolean Expressions of Outputs: Full Adder:**

0

1

1

0

Full adder is a logic circuit that performs binary addition of two 2-bit numbers. It generates two outputs namely ‘**Sum**’ and ‘**Carry**’.

**Truth Table:**

| **A** |  |  | **Carr**  **y** | **B CSum** |
| --- | --- | --- | --- | --- |
| 0 |  |  | 0 0 | 0 |
| 0 |  |  | 0 1 | 0 |
| 0 |  |  | 1 0 | 0 |

0 1 1

| 0 |  |  | 1 1 | 1 |
| --- | --- | --- | --- | --- |
| 1 |  |  | 0 0 | 0 |
| 1 |  |  | 0 1 | 1 |
| 1 |  |  | 1 0 | 1 |
| 1 |  |  | 1 1 | 1 |

0 1 0 0 1

**Boolean Expressions of Outputs:**

or

**Lab Tasks:**

**Question 1(Hardware implementation)**

Design 4x1 MUX using 2x1 MUX

**Question 2: (Hardware implementation)**

Implement the following Boolean function using 4x1 mux.

F (A, B, C, D) Σm (1,4,5,7,9,12,13). consider S1 as A and S0 as B. **Question 3:** Implement 4x1 Mux on trainer using one 2x4 decoder and basic gates **Question 4 (Hardware implementation)**

Implement of full subtractor with a 3x8 decoder and NAND gate. The subtractor inputs are A, B, C. Then subtractor produce outputs D and Bo.

**Question 5 (logic works)**

Implement 8 x1 Mux using one 3 to 8 decoder and basic gates.